IN THE CLAIMS

Claims 1-4 (cancelled)

Claim 5 (previously presented): A method for manufacture of an insulation film for providing an insulation substrate for carrying a semiconductor chip of a semiconductor package comprising the steps of:

providing an insulation film having two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film; and

forming a two-dimensional array of through holes in said insulation film between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*.

Claim 6 (previously presented): The method for manufacture of an insulation film according to claim 5 wherein the pitch L and the pitch p satisfy the following equation: m p = n L wherein n and m are integers that satisfy the equation n < m.

Claim 7 (previously presented): The method for manufacture of an insulation film according to claim 6 wherein the step of forming the through holes further comprises the steps of:

forming the through holes by collective punching out at the effective sprocket hole formation width of the through holes along the transverse direction of the insulation film in a region of length n L along the length-wise direction of the insulation film;

moving the insulation film a length n L in the length-wise direction by means of the sprocket holes; and

repeating these two steps alternately.

Claim 8 (currently amended): The method for manufacture of an insulation film according to claim 6 wherein the method further comprises a step of forming a two-dimensional array of circuit patterns upon the insulation film according to size of the semiconductor package and a ~~for plating electricity supply use~~ conductor pattern electrically connected with the array of circuit patterns.

Claim 9 (currently amended) A method for manufacture of a semiconductor package comprising the steps of: providing an insulation film, forming two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film, forming a two-dimensional array of through holes between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*, forming a two-dimensional plurality of circuit patterns upon the insulation film according to size of the semiconductor package, forming a ~~for plating electricity supply use~~ conductor pattern electrically connected with the plurality of circuit patterns having a main line surrounding a perimeter of the plurality of circuit patterns and a sub-line electrically connecting each of the circuit patterns to the main line;

mounting a semiconductor chip within a respective prescribed region of each circuit pattern of the insulation film and electrically connecting the semiconductor chip with the circuit pattern;

performing resin sealing for partitioning off each region enclosed by the main line of the conductor pattern; and

cutting apart into individual semiconductor packages by dicing along the sub-lines of the insulation film.

Claim 10 (currently amended): The method for manufacture of a semiconductor package according to claim 9 wherein the method further comprises the step of plating each of the circuit patterns upon the insulation film using the ~~for plating electricity supply use~~ conductor pattern.

Claim 11 (currently amended): A method for manufacture of a semiconductor package comprising the steps of: providing an insulation film, forming two rows of

sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film, forming a two-dimensional array of through holes between the rows of sprocket holes, each through hole in said array spaced from adjacent through holes by a pitch *p*, forming a two-dimensional plurality of circuit patterns upon the insulation film according to size of the semiconductor package, forming a conductor pattern electrically connected with the plurality of circuit patterns having a main line surrounding a perimeter of the plurality of circuit patterns and a sub-line electrically connecting each of the circuit patterns to the main line;

mounting a semiconductor chip within a respective prescribed region of each circuit pattern of the insulation film and electrically connecting the semiconductor chip with the circuit pattern;

performing resin sealing for partitioning off each region enclosed by the main line of the conductor pattern; and

cutting apart into individual semiconductor packages by dicing along the sub-lines of the insulation film

~~The method for manufacture of a semiconductor package according to claim 9~~ wherein the dicing step is carried out by use of a dicing blade having a blade trim width wider than the wiring width of the sub-line of the conductor pattern whereby the sub-line is not left behind upon the insulation film.

Claim 12 (currently amended): The method for manufacture of an insulation film according to claim 7 wherein the method further comprises a step of forming a two-dimensional array of circuit patterns upon the insulation film according to size of the semiconductor package and a ~~for plating electricity supply use~~ conductor pattern electrically connected with the plurality of circuit patterns.

Claim 13 (previously presented): A method for manufacture of a semiconductor package comprising the steps of: providing an insulation film, forming two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch *L* along both edges of the insulation film, forming a two-dimensional array of through holes between the rows of sprocket holes, each through hole in said array spaced from adjacent

through holes by a pitch *p*, forming a two-dimensional plurality of circuit patterns upon the insulation film according to size of the semiconductor package, forming a conductor pattern electrically connected with the plurality of circuit patterns having a main line surrounding a perimeter of the plurality of circuit patterns and a sub-line electrically connecting each of the circuit patterns to the main line;

mounting a semiconductor chip within a respective prescribed region of each circuit pattern of the insulation film and electrically connecting the semiconductor chip with the circuit pattern;

performing resin sealing for partitioning off each region enclosed by the main line of the conductor pattern; and

cutting apart into individual semiconductor packages by dicing along the sub-lines of the insulation film,

wherein the method further comprises the step of plating each of the circuit patterns upon the insulation film using the conductor pattern, and

~~The method for manufacture of a semiconductor package according to claim 10~~ wherein the dicing step is carried out by use of a dicing blade having a blade trim width wider than the wiring width of the sub-line of the conductor pattern whereby the sub-line is not left behind upon the insulation film.--

Claim 14 (previously presented): A method of packaging a semiconductor device, comprising the steps of:

providing an insulation film having rows of sprocket holes at a pitch *L* along the edges of said film and a two-dimensional array of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p*;

mounting a semiconductor chip over a number of said through holes;

sealing said semiconductor chip and a portion of said insulation film in resin; and

cutting said insulation film surrounding said semiconductor chip to release said resin-sealed chip from the remainder of said insulation film.

Claim 15 (previously presented): Th m thod of Claim 14, wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional array of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p* and continuously along and transversely across said film within circuit pattern regions on said film.

Claim 16 (previously presented): A method of packaging a semiconductor device, comprising the steps of:

providing an insulation film having rows of sprocket holes at a pitch *L* along the edges of said film and a two-dimensional array of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p*;

mounting a semiconductor chip over a number of said through holes;

sealing said semiconductor chip and a portion of said insulation film in resin; and

cutting said insulation film surrounding said semiconductor chip to release said resin-sealed chip from the remainder of said insulation film,

wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional array of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p* and continuously along and transversely across said film within circuit pattern regions on said film, and

~~The method of Claim 15,~~ wherein said circuit pattern regions are separated by sub-lines of a conductor pattern, and wherein said step of cutting said insulation film comprises cutting said film with a blade having a blade trim width wider than said sub-line is not left behind upon the insulation film after said cutting step.

Claim 17 (previously presented): The method of Claim 14, wherein said step of providing an insulation film comprises:

providing an insulation film having rows of sprocket holes at a pitch L along the edges of said film, and a two-dimensional array of through holes in said film between the rows of sprocket holes, said through holes arranged relative to one another in said array at a pitch *p* and continuously along and transversely across said film.

Claim 18 (previously presented): The method of Claim 14, further comprising the step of depositing solder in selected ones of said number of through holes.

Claim 19 (previously presented): The method of Claim 14, further comprising the step of depositing metal in selected ones of said number of through holes.